Ref. #2
(H07-38815)

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] In the solid state image sensor equipped with the light sensing portion arranged to two-dimensional in the shape of a matrix by making an optoelectric transducer into a pixel, and the horizontal and vertical-scanning circuit for carrying out the address of the optical stored charge signal of each pixel of this light sensing portion one by one, and reading it The shift pulse generating means to which carry out a sequential shift and the single pulse which has fixed pulse width for said vertical-scanning circuit is made to output, Input the shift pulse outputted from this shift pulse generating means, and the pixel line which corresponds synchronizing with the standup and falling of this shift pulse is chosen. The solid state image sensor characterized by constituting from a means to generate the pulse which performs 2nd read-out actuation in the 1st read-out actuation list to the timing from which it differs within a horizontal scanning period at each selection time.
[Claim 2] In the solid state image sensor equipped with the light sensing portion arranged to two-dimensional in the shape of a matrix by making an optoelectric transducer into a pixel, and the horizontal and vertical-scanning circuit for carrying out the address of the optical stored charge signal of each pixel of this light sensing portion one by one, and reading it The shift pulse generating means to which carry out a sequential shift and the pulse which compounded the 1st and 2nd pulses for said vertical-scanning circuit is made to output, Said 1st and 2nd pulses are discriminated from the shift pulse outputted from this shift pulse generating means with a control signal. The solid state image sensor which chooses the pixel line which corresponds synchronizing with each pulse, and is characterized by constituting from a means to generate the pulse which performs 2nd read-out actuation in the 1st read-out actuation list to the timing from which it differs within a horizontal scanning period at each selection time.

[Translation done.]

Ref. #2
(H07-38815)

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is a conceptual diagram for explaining the solid state image sensor concerning this invention.
[Drawing 2] It is a timing chart for explaining actuation of the solid state image sensor shown in drawing 1.
[Drawing 3] They are other conceptual diagrams for explaining the solid state image sensor concerning this invention.
[Drawing 4] It is a timing chart for explaining actuation of the solid state image sensor shown in drawing 3.
[Drawing 5] It is the circuitry Fig. showing the vertical-scanning circuit of the 1st concrete example of the solid state image sensor concerning this invention.
[Drawing 6] It is drawing showing the example of circuitry of the shift register of the vertical-scanning circuit shown in drawing 5.
[Drawing 7] It is drawing having shown the shift register shown in drawing 6 using the symbol.
[Drawing 8] It is a timing chart for explaining actuation of the shift register shown in drawing 6.
[Drawing 9] It is a timing chart for explaining actuation of the vertical-scanning circuit shown in drawing 5.
[Drawing 10] It is drawing showing the example of a configuration of a level mix circuit.
[Drawing 11] It is the circuitry Fig. showing the vertical-scanning circuit of the 2nd example of this invention.
[Drawing 12] It is a timing chart for explaining actuation of the vertical-scanning circuit shown in drawing 11.
[Drawing 13] It is the circuitry Fig. showing the vertical-scanning circuit of the 3rd example of this invention.
[Drawing 14] It is the circuitry Fig. showing the pulse generation section of the vertical-scanning circuit shown in drawing 13.
[Drawing 15] It is a timing chart for explaining actuation of the vertical-scanning circuit shown in drawing 13.
[Drawing 16] It is the circuitry Fig. showing the vertical-scanning circuit of the 4th example of this invention.
[Drawing 17] It is a timing chart for explaining actuation of the vertical-scanning circuit shown in drawing 16.
[Drawing 18] It is the circuitry Fig. showing the vertical-scanning circuit of the 5th example of this invention.
[Drawing 19] It is drawing showing the circuitry of 2 input OR circuit in the pulse generation section of the vertical-scanning circuit of drawing 18, and 2 input AND circuit.
[Drawing 20] It is a timing chart for explaining actuation of the vertical-scanning circuit shown in drawing 18.
[Drawing 21] It is the circuitry Fig. showing the example of a configuration of the conventional CMD solid state image sensor.
[Drawing 22] It is a timing chart for explaining actuation of the CMD solid state image sensor shown in drawing 21.
[Description of Notations]
1 Vertical-Scanning Circuit
2 Horizontal Scanning Circuit
3 Light Sensing Portion
4 Signal Output Terminal
5 Six One-line memory
11, 21, 31, 41, 51 Shift register
12, 22, 32, 42, 52 Pulse generation section
23, 33, 43, 53 Level mix circuit

[Translation done.]

Ref. #2
(H07-38815)

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] Especially this invention relates to the solid state image sensor of the X-Y address type equipped with the function which reads a pixel signal twice independently within an one-frame period about a solid state image sensor.
[0002]
[Description of the Prior Art] In recent years, various kinds of solid state image sensors are developed, and practical use is presented. A CCD mold solid state image sensor, an MOS mold solid state image sensor, a magnification mold solid state image sensor, etc. are typical among these solid state image sensors. As a magnification mold solid state image sensor, what used the charge modulation element (Charge Modulation Device: call for short Following CMD) for JP,60-140752,A, JP,60-206063,A, etc. is indicated. moreover — destructive read in a CMD mold solid state image sensor — T.Nakamura et al., "A New Mos Image Sensor Operating in a Nondestructive Readout Mode", and IEDM Dig.Tech.Papers p.353 (1986) etc. — it is indicated in detail.
[0003] Each of these solid state image sensors arranges the pixel which has a photo-electric-conversion function in the shape of a matrix, and in the CCD mold solid state image sensor, they is constituted by the charge transmittal mode so that a pixel may be scanned and a video signal may be read by the X-Y addressing method in an MOS mold solid state image sensor and a magnification mold solid state image sensor. For this reason, in these solid state image sensors, after fixed time amount exposure of each pixel which constitutes a solid state image sensor is carried out, it scans sequentially, and the pixel signal for one screen is outputted with this scan.
[0004] Next, the example of a configuration of a CMD solid state image sensor is explained as an example of the conventional solid state image sensor. Drawing 21 is drawing showing the circuitry of a CMD solid state image sensor. CMD 111-11,111-12 and ... which constitute each pixel — 111-mn is arranged in the shape of a matrix, and the video electrical potential difference VDD (> 0) is impressed to each of that drain in common. the gate terminal of the CMD group of each line arranged in the direction of X — line Rhine 112-1, 112-2, and ... 112-m the source terminal of the CMD group of each train which connected, respectively and was arranged in the direction of Y — train Rhine 113-1, 113-2, and ... 113-n It connects, respectively. and train Rhine 113-1, 113-2, and ... 113-n — respectively — the transistor 114-1 for train selection, 114-2, and ... 114-n and the transistor 115-1 for anti-selection, 115-2, and ... 115-n minding — video line 116 And Rhine 117 grounded by GND It connects in common, respectively. video line 116 Pre amplifier 122 of the current-electrical-potential-difference conversion mold with which the imaginary earth of the input was carried out it connects — having — pre amplifier 122 Output terminal 119 **** — the video signal of negative polarity is read by time series.
[0005] moreover, line Rhine 112-1, 112-2, and ... 112-m Vertical-scanning circuit 120 It connects. It is a signal phiG1 and phiG2, respectively... phiGm is impressed. moreover, the transistor 114-1 for train selection, 114-2, and ... 114-n and the transistor 115-1 for anti-selection, 115-2, and ... 115-n A gate terminal Horizontal scanning circuit 121 It connects and is a signal phiS1 and phiS2, respectively... phiSn and those reversal signals are impressed. furthermore, vertical-scanning circuit 120 The bias terminal V1, V2, V3, and V4 **** — the are recording electrical potential difference VINT, the read-out electrical potential difference VRD, the reset electrical potential difference VRS, and the overflow electrical potential difference VOF are impressed, respectively.
[0006] Drawing 22 is a signal waveform diagram for explaining actuation of the CMD solid state image sensor

shown in drawing 21. line Rhine 112-1, 112-2, and ... 112-m the signal phiG1 to impress, phiG2, and ... phiGm Read-out gate voltage VRD, the reset electrical potential difference VRS, the overflow electrical potential difference VOF, and are recording electrical potential difference VINT Become and it sets in a non-choosing line. It is set to VOF during VINT and a horizontal blanking interval during a level image shelf-life, and is set to VRS during VRD and a horizontal blanking interval during a level image shelf-life in a selection line. moreover, the transistor 114-1 for train selection, 114-2, and ... 114-n The signal phiS1 impressed to a gate terminal, phiS2, ... phiSn train Rhine 113-1,113-2 and ... 113-n By the signal for choosing "L" level -- the transistor 114-1 for train selection, 114-2, and ... 114-n OFF the transistor 115-1 for anti-selection, 115-2, and ... 115-n It sets to ON. "H" level -- the transistor 114-1 for train selection, 114-2, and ... 114-n ON -- carrying out -- the transistor 115-1 for anti-selection, 115-2, and ... it is set up so that it may become the electrical-potential-difference value which makes 115-n off.

[0007] Moreover, it sets to what was constituted so that the pixel signal for the horizontal direction of one line could be held as indicated by JP,4-86166,A. During a level image shelf-life, during VOF and a horizontal blanking interval, it sets [in / in order to take out the pixel signal which performed maintenance actuation of a pixel signal during the horizontal blanking interval, and was held during the level image shelf-life / a selection line] in VRD or VRS, and a non-choosing line, and is VINT. It is constituted so that it may become.

[0008]

[Problem(s) to be Solved by the Invention] By the way, in the solid state image sensor of the above-mentioned configuration, when rationalization of exposure conditions is made by a shutter etc., for example to the bright part of a photographic subject, the light exposure in the pixel equivalent to the dark part of a photographic subject becomes small, and it becomes easy to be influenced of noises, such as random noise which the solid state image sensor itself generates, and a fixed pattern noise. On the other hand, when rationalization of exposure conditions is made to the dark part of a photographic subject, it becomes exaggerated exposure and a pixel signal is saturated with the pixel equivalent to the bright part of a photographic subject. This is because only the pixel signal of the exposure time of all pixel identitases is acquired once by one frame in the conventional solid state image sensor.

[0009] This invention was made in order to cancel the above-mentioned trouble in the conventional solid state image sensor, and it aims at offering the solid state image sensor which can acquire independently the pixel signal with which two sorts of exposure times differ within an one-frame period.

[0010]

[Means for Solving the Problem and its Function] The light sensing portion which this invention made the optoelectric transducer the pixel and was arranged to two-dimensional in the shape of a matrix in order to solve the above-mentioned trouble, In the solid state image sensor equipped with the horizontal and vertical-scanning circuit for carrying out the address of the optical stored charge signal of each pixel of this light sensing portion one by one, and reading it The shift pulse generating means to which carry out a sequential shift and the single pulse which has fixed pulse width for said vertical-scanning circuit is made to output, Input the shift pulse outputted from this shift pulse generating means, and the pixel line which corresponds synchronizing with the standup and falling of this shift pulse is chosen. [whether it constitutes from a means to generate the pulse which performs 2nd read-out actuation in the 1st read-out actuation list to the timing from which it differs within a horizontal scanning period at each selection time, and] Or the shift pulse generating means to which carry out a sequential shift and the pulse which compounded the 1st and 2nd pulses is made to output, Said 1st and 2nd pulses are discriminated from the shift pulse outputted from this shift pulse generating means with a control signal. The pixel line which corresponds synchronizing with each pulse is chosen, and it constitutes from a means to generate the pulse which performs 2nd read-out actuation in the 1st read-out actuation list to the timing from which it differs within a horizontal scanning period at each selection time.

[0011] Thus, in the constituted solid state image sensor, synchronizing with the standup and falling of a single pulse which have the fixed pulse width which shifts the inside of a vertical-scanning circuit, a pixel line is chosen synchronizing with the 1st and 2nd pulses, and 1st read-out actuation and 2nd read-out actuation are performed to the timing from which it differs within a horizontal scanning period at each selection time. The solid state image sensor which can acquire independently the pixel signal with which two sorts of exposure times differ within an one-frame period by this is realizable.

[0012] Next, this invention is further explained to a detail using a conceptual diagram. Drawing 1 is a conceptual diagram for explaining the solid state image sensor concerning this invention. In drawing, 1 is the light sensing portion which a vertical-scanning circuit and 2 made the optoelectric transducer as the horizontal scanning

circuit, and 3 made the pixel, and was arranged to two-dimensional in the shape of a matrix. The vertical-scanning circuit 1 shows the mode in the case of the 1st and 2nd read-out actuation shifting by n lines, and operating by the conceptual diagram which outputted the 1st and 2nd read-out signals with which timing differs within a level shelf-life, and was shown in drawing 1 .

[0013] Drawing 2 is a timing chart which shows actuation of the solid state image sensor shown in drawing 1 . 1-1, 1-2, 1-3, and ... 1-n It is the scan pulse outputted from the vertical-scanning circuit 1, and read-out actuation of a period and a pixel signal which serves as "H" level to the timing from which it differs within a level shelf-life at intervals of nH, and serves as "H" level is performed. ** shows the 1st read-out timing and ** shows the 2nd read-out timing here. If a start signal is twice inputted into the horizontal scanning circuit 2 of drawing 1 within a level shelf-life as HST of drawing 2 shows when such a pulse is outputted from the vertical-scanning circuit 1, in the signal output terminal 4, a pixel signal will appear to the timing shown by Sig. The part which expresses the pixel signal of how many lines the figure shown in Sig. is, and attaches the slash shows the pixel signal of read-out of the 2nd. The pixel signal in read-out of the 1st and the 2nd can be treated independently here, without being mixed.

[0014] Next, the solid state image sensor concerning this invention is explained using other conceptual diagrams shown in drawing 3 . Unlike what was shown in drawing 1 , the solid state image sensor shown in this conceptual diagram reads and holds a pixel signal at a horizontal blanking interval, and it constitutes it so that it may take out outside at a level shelf-life. A different point from what was shown in drawing 1 in the solid state image sensor shown in drawing 3 is a point which has the memory for holding the pixel signal for one line by two lines, is 5 here about the 1st one-line memory at the time of the 1st read-out actuation, and shows the 2nd one-line memory at the time of the 2nd read-out actuation by 6.

[0015] the pulse 1-1 which drawing 4 is the timing chart which shows actuation of the solid state image sensor shown in drawing 3 , and is outputted from the vertical-scanning circuit 1, 1-2, 1-3, and ... read-out actuation of a pixel signal is performed at the period which serves as "H" level to the timing from which it differs within a horizontal blanking interval at intervals of nH, and serves as this "H" level, and 1-n is held at the one-line memory 5 and 6. Then, if a start pulse as shown in the horizontal scanning circuit 2 by HST is given, in the signal output terminal 4-1 and 4-2, a pixel signal will appear at a level shelf-life to the timing shown by Sig.1 and Sig.2.

[0016] Also in which solid state image sensor shown in above-mentioned drawing 1 and drawing 3 , since time amount is shifted and two read-out actuation is performed, especially the pixel signal in each read-out actuation can take out independently the perpendicular signal line in a light sensing portion 3 in the conventional state, without preparing more than one.

[0017]

[Example] Next, a concrete example is explained. Drawing 5 is the circuitry Fig. showing the configuration of the vertical-scanning circuit which is the principal part of the 1st example of the solid state image sensor equipped with the function which reads a pixel signal twice independently within the one-frame period concerning this invention. The vertical-scanning circuit in this example consists of a shift register 11 and the pulse generation section 12.

[0018] Next, the shift register 11 used for the above-mentioned vertical-scanning circuit is explained using drawing 6 . This shift register 11 constitutes 1 unit 11U enclosed with a drawing destructive line with four steps of clocked inverters, as shown in drawing 6 . When this shift register is shown using a symbol, it is expressed as shown in drawing 7 . In drawing 6 and drawing 7 , VCK1, VCK2, *VCK1, and *VCK2 are clocks which drive a shift register, and *VCK1 and *VCK2 show the reversal clock of VCK1 and VCK2, respectively. Moreover, VST is a start pulse.

[0019] Drawing 8 is a timing chart for explaining actuation of the shift register 11 shown in drawing 6 and drawing 7 . the first rank of a shift register — by impressing a start pulse VST to the input of a unit, output Sn-m (n= 1, 2, ..., m= 1, 2, 3, 4) appears synchronizing with a clock VCK1 or falling of VCK2. Sn-m (n= 1, 2, ..., m= 1, 2, 3, 4) shows the n-th step of output [the m-th step of] of a clocked inverter of a shift register unit here.

[0020] In drawing 5 , when unit unit 12U of the pulse generation section 12 consists of one inverter, two 2 inputs OR, and one 2 input NAND and logical expression expresses the n-th step of output Pn, it is expressed with several 1.

[0021]

[Equation 1]

$$Pn = \overline{\{(Sn-2) + \overline{(Sn-4)}\} \cdot \{(S(n+1)-1) + (S(n+1)-2)\}}$$
$$= \{\overline{(Sn-2)} \cdot (Sn-4)\} + \{\overline{(S(n+1)-1)} \cdot \overline{(S(n+1)-2)}\}$$

[0022] Sn-m (n= 1, 2, ..., m= 1, 2, 3, 4) expresses the output of a shift register here. As one above shows, the conditions from which the pulse generation section output Pn serves as "H" level are the following two kinds. (1)-1: For Sn-2, both "L" level and (Sn-4) "H" level (1)-2: (S (n+1)-1) and (S (n+1)-2) are "L" level [0023]. Drawing 9 is a timing chart for explaining actuation of the vertical-scanning circuit of a configuration of having been shown in drawing 5 . The driving pulse of a shift register 11 and VST are the start pulses of a shift register 11, and VCK1 and VCK2 have a certain width of face. S1-4 - S4 -4 are the outputs of a shift register 11, and synchronize with falling of VCK1 or VCK2. P1-P4 are the outputs of the pulse generation section 12. It explains here paying attention to the 2nd step of output P2 of the pulse generation section.

[0024] Setting to the standup timing of shift pulse S2-4, condition (1)-2 to the pulse generation section output P2 is t1 -t2. In a period, since both shift pulse S3-1 and S3-2 are set to "L" level, it is set to "H" level. Moreover, it sets to falling timing and is condition (1)-1 to t3 -t4. In a period, since shift pulse S2-2 are set to "L" level and S2-4 are set to "H" level, the pulse generation section output P2 serves as "H" level. It is period t1 -t2 here. t3 -t4 do not overlap within 1 horizontal-scanning period.

[0025] Therefore, read-out of the 1st is performed in the standup of a shift pulse, and read-out of the 2nd is performed in falling. By read-out of the 1st, the exposure time in each read-out turns into time amount equivalent to "L" level period of a shift pulse, and turns into time amount equivalent to "H" level period of a shift pulse by read-out of the 2nd.

[0026] Moreover, T2 in the driving pulse VCK1 shown in drawing 9 Since read-out of the 1st and the 2nd is performed within a period, either a level shelf-life or a horizontal blanking interval can perform read-out of the 1st and the 2nd by control of the timing of the driving pulse of a shift register 11.

[0027] As explained above, according to the vertical-scanning circuit of a configuration of having been shown in drawing 5 , in the standup and falling of a shift pulse, 1st and 2nd read-out actuation can be performed to the timing from which it differs within a horizontal scanning period, and it can apply to the solid state image sensor of an X-Y addressing method.

[0028] Next, the vertical-scanning circuit at the time of applying this invention to the image sensors using the CMD photo detector which is a magnification mold solid state image sensor as the 2nd example is explained. When making a video signal output from a CMD photo detector, as a signal impressed to the common gate line of each line of the CMD photo detector arranged in the shape of a two dimensional array, the pulse signal which combined four electrical potential differences, the are recording electrical potential difference VINT, the overflow electrical potential difference VOF, the read-out electrical potential difference VRD, and the reset electrical potential difference VRS, with time series is needed. In order to impress such a signal to the gate of a CMD photo detector, the vertical-scanning circuit equipped with the circuit and level mix circuit of a configuration of that fanout binary [of selection / not choosing] is obtained from each scan stage is used.

[0029] As a level mix circuit, there is a thing of the circuitry shown in drawing 10. In drawing 10, S is a signal which is un-choosing on selection and "H" level with "L" level. RD/RS is the binary signal of VRD and VRS, and when S is "L" level, VRD or VRS is outputted. When S is "H" level, on the other hand, it synchronizes with Clock phi, and they are VOF or VINT. It is outputted and the gate line impression signal G of 4 value level is acquired. In addition, *phi is the reversal clock of phi.

[0030] Drawing 11 is drawing showing the circuitry of the vertical-scanning circuit of the 2nd example. The differences from the vertical-scanning circuit of the 1st example shown in drawing 5 are having formed the level mix circuit 23 explained by drawing 10, and the point that several 1 and logic are [the output of the pulse generation section 22] reverse since "L" level is chosen when this level mix circuit 23 is used.

[0031] Drawing 12 is a timing chart for explaining actuation of the vertical-scanning circuit shown in drawing 11. VCK1 and VCK2 are the driving pulses of a shift register 21. VCK10 is the overflow electrical potential difference VOF and the are recording electrical potential difference VINT which are used for the level mix circuit 23. It is the clock which determines timing and is the binary signal of the read-out electrical potential difference VRD and the reset electrical potential difference VRS which also uses RD/RS for the level mix circuit 23. VST is the start pulse of a shift register 21, and S1-4-S3-4 are the output of a shift register 21. P1-P3 are the

outputs of the pulse generation section 22, and the timing used as "L" level is the same as the timing used as "H" level of the 1st example shown in drawing 9 . If the outputs P1-P3 of these pulse generation sections are given to the level mix circuit 23, a RD/RS signal will appear in the output G1 of the period when P1-P3 are set to "L" level, and the level mix circuit 23 - G3. And read-out actuation is performed at the period used as the read-out electrical potential difference VRD, and a reset action is performed at the period used as the reset electrical potential difference VRS. On the other hand, the period P1-whose P3 are "H" level synchronizes with VCK10, and is the overflow electrical potential difference VOF or the are recording electrical potential difference VINT. It appears in an output G1 - G3. In addition, in drawing 12, ** shows the 1st read-out timing, and ** shows the 2nd read-out timing, and the exposure time of a signal [in / in Tint1 / the 1st read-out timing] and Tint2 show the exposure time of the signal in the 2nd read-out timing.

[0032]